PATENT APPLICATION

# METHOD AND APPARATUS FOR TRANSMITTING DATA IN A PUBLIC NETWORK

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5    METHOD AND APPARATUS FOR
TRANSMITTING DATA IN A PUBLIC NETWORK

BACKGROUND OF THE INVENTION

The present invention relates to transmission of
10   data on a subscriber loop in a public network such as, for
example, a telephone network.  More specifically, the present
invention provides an improvement of standard single-line
digital subscriber line (SDSL) technology.

A wide variety of technologies and transmission
15   standards have been developed for transmission of data via
currently existing public network resources.  The term
"digital subscriber line" refers to a modem or modem pair
connected by one or more twisted pairs having a specific data
frame format and associated transmission rate.  The first
20   digital subscriber line technology, referred to as IDSL,
corresponds to what is also known as basic rate ISDN.  IDSL
technology transmits duplex data at 144 kbps over copper lines
using a 2B1Q modulation scheme.  The modems multiplex and
demultiplex the data stream into two B channels (64 kbps each)
25   and a D channel (16 kbps) as described in ANSI T1.601, the
entirety of which is incorporated herein by reference for all
purposes.

High data rate digital subscriber lines (HDSL) are
related to the earlier IDSL using the same modulation scheme
30   to transmit data at the T1 data rate over two twisted pairs as
described in ANSI Committee T1 TR-28 and ETR 152, the
entireties of which are incorporated herein by reference for
all purposes.  A single line digital subscriber line (SDSL) is
a single pair version of HDSL, i.e., transmitting data at one-
35   half the T1 data rate, i.e., 768 kbps, over a single twisted
pair.

For both HDSL and SDSL and as shown in Fig. 1, data
are organized into 6 ms frames 102 comprising alternating
overhead and payload sections 104 and 106.  The four payload
40   sections 106 each include twelve 97-bit payload blocks 108, 96

bits (110) of which are data and one bit (112) of which is known as the F/Z bit. This works out to the well known SDSL data rate of 768 kbps. Overhead sections 104 along with bits 112 represent an additional 16 kbps for an actual line rate of
5    784 kbps.

      Fig. 2 is a simplified block diagram of a standard SDSL 202 connecting a central office or public branch exchange (represented by modem 204) and a subscriber premises (represented by modem 206). The data to be transmitted enters
10   framing circuitry 208 of modem 204 at the raw data rate of 768 kbps. Framing circuitry 208 organizes the incoming data stream into the 6 ms frames described above with reference to Fig. 1 using a 768 kHz oscillator 210 and frame overhead data generated at 16 kbps. The framed data are then sent to bit
15   pump 212 where, using a 784 kHz oscillator 214, they are encoded according to the 2B1Q modulation scheme and transmitted via twisted pair 216 to the subscriber premises as represented by modem 206.

      At the subscriber premises, the modulated framed
20   data are received at the rate of 784 kbps and demodulated by bit pump 218 which is clocked by a 784 kHz oscillator 220. The demodulated data are then received by framing circuitry 222 which strips off the 16 kbps frame overhead data and decomposes the 6 ms HDSL frames into a 768 kbps data stream.
25   Framing circuitry 222 is clocked by a phase-locked loop (PLL) recovered clock (PLL circuitry 224) derived from the incoming data stream.

      The F/Z bit in each payload block (field 112 of Fig. 1) is reserved for use with standard T1 and E1 <u>for loop</u>
30   <u>identification and out-of-band signaling</u> for the transmission of special alarm codes which are only applicable to T1 and E1 <u>transmissions</u>. When standard framing circuitry receives a standard frame, the F/Z bit information is written to an F/Z bit register associated with the framing circuitry. If the
35   transmission is a T1 or E1 transmission, the F/Z bit data are then used in accordance with their intended purpose according to well known techniques. However, when a data frame is on a network link which uses only SDSL technology and does not

interface with T1 or E1 technology, the F/Z bit register and the data stored therein are ignored representing 8 kbps of wasted bandwidth.  This may seem a relatively small amount of bandwidth with reference to the standard rate of 768 kbps.

5  However, when viewed relative to the subject matter described in commonly assigned, copending U.S. Patent Application No. 09/107,840 for METHODS AND APPARATUS FOR TRANSMITTING DATA IN A PUBLIC NETWORK filed simultaneously herewith, the entire specification of which is incorporated herein by reference for

10  all purposes, such a small bandwidth increase becomes more important.  That is, the above-referenced copending application describes methods and apparatus by which the current HDSL data transmission infrastructure may be leveraged to provide lower effective data rates than the standard 768

15  kbps without sacrificing the advantages of the standard frame format.  At the lower transmission rates made possible by those techniques, an extra 8 kbps could prove extremely valuable.

It is therefore desirable to provide data

20  transmission techniques which avoid wasting this valuable data bandwidth on SDSL transmission links while retaining the compatibility advantages of the standard frame.


SUMMARY OF THE INVENTION

25  According to the present invention, the F/Z bits in the payload blocks of standard HDSL frames are used to transmit data over SDSL links which do not interface with T1 or E1 links, i.e., links on which the F/Z bits are employed for their intended purpose.  Instead of ignoring the F/Z bit

30  data and the F/Z bit registers, the present invention uses them for an additional 8 kbps of data throughput.  As discussed above, this is a fairly small incremental improvement relative to a data rate of 768 kbps.  However, when viewed relative to the variety of SDSL data rates made

35  possible by the techniques described in the above-referenced patent application, an additional 8 kbps can provide an even higher degree of flexibility for service providers with regard to the number of data rate options they can offer subscribers.

Moreover, as mentioned above, an 8 kbps increase in data throughput is much more significant for the lower SDSL data rates made possible by such technology.

Thus, the present invention provides a method and apparatus for transmitting data in a network between first and second single-line digital subscriber line (SDSL) modems using a standard high data rate digital subscriber line (HDSL) frame format. The frame format includes at least one field in each data payload block, e.g., the F/Z bit field, for implementing a feature relating to one of the T1 and E1 transmission protocols. According to the invention, the at least one field is employed for transmission of selected payload data.

According to a specific embodiment, selected payload data are taken from the data stream received by the first SDSL modem and stored in a register associated therewith. The register corresponds to the T1/E1 protocol feature. The selected payload data in the register are then used to generate a sequence of data frames wherein the selected payload data occupy the at least one field in the data payload blocks.

According to another embodiment, selected payload data are taken from the at least one field in the payload blocks of the sequence of data frames received by the second SDSL modem and stored in a register associated therewith. The register corresponds to the T1/E1 protocol feature. The selected payload data in the register are then inserted into the data stream

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified block diagram of a standard HDSL frame format;

Fig. 2 is a simplified block diagram of a standard SDSL connecting a central office or public branch exchange and a subscriber premises; and

Fig. 3 is a simplified block diagram of an SDSL

connecting a central office or public branch exchange and a
subscriber premises according to a specific embodiment of the
invention.

5               DESCRIPTION OF SPECIFIC EMBODIMENTS
                Fig. 3 is a simplified block diagram of an SDSL 302
connecting a central office or public branch exchange
(represented by modem 304) and a subscriber premises
(represented by modem 306) according to a specific embodiment
10    of the invention.  According to a specific embodiment, the
data to be transmitted enters framing circuitry 308 at the raw
data rate of 776 kbps, i.e., 8 kbps more than the standard
HDSL rate of 768 kbps.  It will be understood however that,
according to the techniques described in the above-referenced
15    copending application and as noted in Fig. 3, data may enter
the subscriber loop at a variety of rates, i.e., $(n + 8)$ kbps,
where n represents a data rate without the improvement
described herein, without departing from the scope of the
present invention.  That is, the present invention may be used
20    to increase by 8 kbps the data throughput for any SDSL
transmission link regardless of the data rate (n) of that link
without the improvement.  According to specific embodiments of
the invention, framing circuitry 308 may be based on, for
example, the Brooktree Bt8953A Channel Unit or the Level One
25    SK70720 MDSL Framer chip.
                Using 16 kbps of frame overhead data, framing
circuitry 308 organizes the incoming data stream into frames
which are structured similarly to those described above with
reference to Fig. 1 with an important distinction.  Some of
30    the bits in the incoming raw data stream are directed to the
F/Z bit register associated with framing circuitry 308.  This
is accomplished using the flexible programmable features of
the framing circuitry chip set.  This is possible due to the
fact that, because SDSL technology makes no use of this
35    register, there is no competing F/Z bit data to be stored in
the register.  Then, because these bits are in the F/Z bit
register, they are included in the data frames generated by
framing circuitry 308 in the F/Z bit slot in each of the

frame's payload blocks.  That is, the data bits stored in the
F/Z bit register occupy the same position in the generated
data frames as the F/Z bits would have occupied if the data
were being transmitted according to the T1 or E1 protocol.

5          Thus, according to the invention, a higher effective
data rate is made possible while keeping all frame parameters
the same as for standard HDSL/SDSL transmission.  Maintaining
the standard frame helps to ensure that the transmitted frames
are compatible with any hardware they are likely to encounter.

10    Framing circuitry 308 employs clock circuitry 310 to
synchronize with the incoming data stream.  Clock circuitry
310 may be implemented in a variety of ways.  According to
specific embodiments, clock circuitry 310 is implemented as
described in the above-referenced copending patent

15  application.

          The framed data are then sent to bit pump 312 where,
using clock circuitry 314, they are encoded according to the
2B1Q modulation scheme and transmitted via twisted pair line
316 to the subscriber premises as represented by modem 306.

20  Clock circuitry 314 generates a clock signal which is 16 kHz
greater than the frequency generated by clock circuitry 310 to
account for the 16 kbps of frame overhead.  This is denoted
with the term (64n + 24) kHz.  As discussed above with
reference to clock circuitry 310, clock circuitry 314 may be

25  implemented according to a variety of techniques.

          According to a specific embodiment, clock circuitry
310 and 314 are provided according to the techniques described
in commonly assigned, copending U.S. Patent Application No.
*Patent No. 6,195,385*
09/109,991 for HTU-C CLOCKING FROM A SINGLE SOURCE filed

30  simultaneously herewith, the entire specification of which is
incorporated herein by reference for all purposes.

          At the subscriber premises, the modulated framed
data are received and demodulated by bit pump 318 which is
clocked by clock circuitry 320 at the same rate as clock

35  circuitry 314.  As with clock circuitry 310 and 314, clock
circuitry 320 may be implemented according to a variety of
techniques.  The demodulated data are then received by framing
circuitry 322 which strips off the 16 kbps frame overhead data

and decomposes the 6 ms HDSL frames into the original n + 8 kbps data stream. Framing circuitry 322 is clocked by a phase-locked loop (PLL) recovered clock (PLL circuitry 324) derived from the incoming data stream.

5        Framing circuitry 322 may be based on the HDSL chips sets described above with reference to framing circuitry 308. As with framing circuitry 308, the chip set upon which framing circuitry 322 is based is programmed to use rather than ignore the F/Z bit data. The F/Z bit data is stored in

10 the F/Z bit register and then inserted into the reconstructed data stream. Again, this is made possible by the flexible programmability of the chip set upon which framing circuitry 322 is based.

        While the invention has been particularly shown and

15 described with reference to specific embodiments thereof, it will be understood by those skilled in the art that changes in the form and details of the disclosed embodiments may be made without departing from the spirit or scope of the invention. For example, one specific embodiment described above results

20 in a data rate of 776 kbps, i.e., 8 more than the HDSL standard of 768 kbps. It will be understood, however, that the present invention may be employed to achieve an 8 kbps increase over the other HDSL standard rates of 1152 and 2304 kbps, i.e., 1160 and 2312 kbps, respectively. Therefore, the

25 scope of the invention should be determined with reference to the appended claims.